

MEG II 実験背景事象削減のための 高レート耐性RPCの高抵抗電極の開発 -設計と製作-

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Outline

➤Introduction

- MEG II experiment
- Radiative decay counter
- RPC for upstream RDC
- Status of studies with prototype

Development of a new pillar structure

- Problem of pillar formation
- New strategy for obtaining sufficient gap
- Alignment method

Development of resistive electrode

- Rate capability of RPC
- Suppression of voltage drop
- Determination of strip pitch
- Implementation of HV supply

Summary and prospect

MEG II experiment

►MEG II searches for $\mu^+ \rightarrow e^+ \gamma$ decay

Charged lepton flavor violating decays

>Main Background source is accidental coincidence of BG- e^+ and BG- γ



Radiative Decay Counter (RDC)

> Detector for tagging BG- γ

- When BG- γ have a signal-like energy (~ 52.8 MeV), most of e⁺ have a low energy (1-5 MeV)
- Downstream RDC has already been installed
- Upstream RDC is under development

➢Requirements to upstream RDC

Material budget: < 0.1% radiation length

> 90%

< 1 ns

- \Rightarrow muon beam with 28 MeV/c must pass through the detector
- 2. Rate capability:

1.

- 3. Radiation hardness: > 60 weeks operation
- 4. MIP efficiency:
- 5. Timing resolution:
- 6. Detector size: 20 cm (diameter)



 4 MHz/cm^2 of muon beam





RPC for upstream RDC

- **RPC** → **Fast response** (< 1 ns)
- DLC
 Controllable resistivity (by changing film thickness)
 Small material budget (by sputtering directly onto thin polyimide films)

Al readout strip >MEG II RPC design \rightarrow 4-layer RPC (**30 nm**) +HVMaterial budget DLC (~100 nm) • Polyimide 50 μ m \rightarrow 0.018% X_0 **Polyimide foil** • Aluminum 30 nm \rightarrow $0.0034\% X_0$ (50 µm) 0.095% radiation length Achieved < 0.1% radiation length Spacer (300-400 µm) -HV φ20 cm

Status of studies with prototype

> Previous research reports with 3 cm \times 3 cm prototype RPC

MIP Efficiency

The n-layers RPC efficiency is

 $\epsilon_n = 1 - (1 - \epsilon_1)^n$ ϵ_n : n-layer efficiency

- $ightarrow \epsilon_1 > 40\%$ required for > 90% efficiency
- 60% MIP efficiency is achieved with single-layer RPC

• 90% MIP efficiency

is achievable with 4-layer RPC

Timing resolution

Achieved 160-170 ps

with $384 \ \mu m$ gap single-layer RPC



Today's talks

About manufacturing

>Pillar formation using new material

New design for obtaining wide gap spacing in RPC

> Development of resistive electrode to achieve rate capability

- $\boldsymbol{\cdot}$ Implement HV supply geometry \rightarrow This talk
- Control of DLC resistivity \rightarrow Next talk

RPC with DLC electrodes

Spacer

DLC electrodes

Problem of pillar formation

Pillar formation by photolithography technology

- The previous pillar material is no longer available
 - Use new pillar material

DuPont[™] Pyralux[®] → Solder resist

Pillar formation test

- 100 μm -thick on DLC
 - Done w/o any problem
- \bullet 300 μm -thick on Cu
 - Done w/ non-flatness of pillars
- 350 μm -thick on Cu
 - Failed due to the difficulties reported
 - Increased development time
 → Many pillars tilted or missing



- Upper side: Inverse trapezoidal shape due to the amount of transmission during exposure
- Lower side: Photoresist remains due to insufficient development.

New strategy for obtaining sufficient gap

- ≻Formable up to 300 µm-thick
 - ➡ Not expected to have sufficient detection efficiency
- $\succ 200~\mu m$ -thick pillars are attached on the both sides



Alignment method

Alignment by alignment holes and pins



Alignment accuracy

- Mask formation:
- $\sim 1 \, \mu m$ (negligible)
- Work by laser:

- < **50 µm** (20 µm at best)
- Alignment of both sides: $< 50 \ \mu m$

Effect of misaligned pillars to be test

- Electric field structure
- RPC operations



Today's talks

About manufacturing



Development of resistive electrode to achieve rate capability

- Implement HV supply geometry → This talk
- Control of DLC resistivity \rightarrow Next talk

Rate capability

➢Rate capability of RPC



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 $\rho_{\rm S} = 7 \ {\rm M}\Omega/{\rm sq}$

Suppression of voltage drop



>HV supply geometry (reported JPS2021-autumn)

- The distance from HV supply must be small
 strip geometry
 - In addition, the strip geometry allows for larger detector





Larger δV with larger distance

Large detector w/ HV strips

Determination of strip pitch



- The strip becomes an inactive region
 Too narrow pitch is bad
- $\cdot \, \delta \mathrm{V}$ dependency on ℓ_{pitch}
 - Calculated using the above equation
 - $\boldsymbol{\cdot}$ Optimal $\boldsymbol{\ell}_{pitch}$ depends on surface resistivity

In order to achieved $\delta V < 100V$,

ℓ_{pitch} = 1 cm is required
 ➡ Implement conductive strips for HV supply



Voltage drop ($\rho_S = 10 \text{ M}\Omega/\text{sq}$)



Implementation of HV supply

- Material for conductive strips
 - Use chromium for conductive strips
 - Easy to bond to DLC
 - Other metals are difficult to bond to DLC
 - $\boldsymbol{\cdot}$ The chrome strip is covered with an insulator
 - Prevention of discharge
- Chromium sputtered on DLC (lift-off method)
 - Determination of strip width
 - As thin as possible to reduce inactive area
 - Masking and alignment accuracy
 - → Inactive area: 2.1 % for a detector with ϕ 20 cm

Prototype using the improved electrode is now in production



	Conductive strips	Insulation cover
Material	Chromium	Dry resist
Thickness	100 nm	25 μm
Width	50 µm	200 µm

Summary and prospect

High-rate capable RPC with DLC electrodes is under development for MEG II upstream RDC

Development of a new pillar structure

- 0.2 mm-thick pillars are attached on the both sides
- · Electrodes are accumulated with precise alignment

> Development of electrodes for improving rate capability

- Implementation of conductive strips for HV supply
 - · Use chromium as conductive strips and protected by insulating cover
- Prototype is now in production

Planned studies

- · Rate capability test using improved electrodes in this year
 - If performance can be demonstrated with a prototype, the requirements can be achieved with a large detector

Backups

RMD e⁺ distribution





Status of rate capability studies

$\nabla^2 \delta \mathbf{V}(x, y) = \boldsymbol{Q}_{\text{mean}}(\mathbf{V}_{\text{eff}}) \cdot \boldsymbol{f}(x, y) \cdot \boldsymbol{\rho}_S$

Avalanche charge

Surface resistivity

Known parameters (reported in JPS2021-autumn)

- \cdot Requirements to δV : < 100 V
 - \rightarrow Determined by the voltage achieved > 50% with single-layer
- Avalanche charge: measured for low-momentum muon beam

Hit rate

• Hit rate: 4 MHz/cm^2 at the center



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Voltage drop of RPC



>The voltage drop due to high current on resistive electrodes

- Current paths are different between conventional and surface type
- ➡ In surface RPC, the distance between conductors affects voltage drop

Diamond-Like Carbon (DLC)

>Amorphous structure with graphite (sp^2) and diamond (sp^3) bonds

- sp²: Electrically conductivity
- sp³: Insulating properties
- ➢Features:
 - · High-definition patterning (< 10 $\mu m)$
 - Wide range of surface resistivity can be set (50 $k-3~\text{G}\Omega/\text{sq})$
 - Film thickness adjustment
 - Nitrogen doping
 - · High adhesion to polyimide
 - · Chemically stable



Comparison of diamond, DLC and graphite structures Ref) <u>https://nippon-itf.co.jp/technical/article/about-dlc.html</u>

Sputtering technology

Sputtering Method

- 1. Inert gas (mainly Ar) is added in a vacuum
- Apply a negative charge to the deposition material
 ➡ lonizes gas atoms by causing glow discharge
- 3. Gas ions collide with target at high velocity
- 4. The beaten-up target constituent particles adhere to and deposit on substrate surface
 ➡ Thin film formation



Pillar formation using photoresist

1. Masked and exposed with UV light



2. Dissolve non-exposed areas with developer



3. Pillar is completed



4. Heat harden (Baking)



Pillar formation

>Inverse trapezoidal shape

due to the amount of transmission during exposure



Photoresist remains due to insufficient development

