

An FPGA-based trigger for the search of $\mu^+ \rightarrow e^+ \gamma$ decay in the MEG experiment

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Abstract—A novel trigger has been set up and it is now operating in the MEG experiment at Paul Scherrer Institut, which aims at searching for the Lepton Flavour violating decay $\mu^+ \rightarrow e^+ \gamma$ with unprecedented sensitivity (10^{-13} for the branching ratio). An overview of the trigger architecture is given, as well as a description of the design and the main features of the dedicated boards and their usage. Particular emphasis is laid on the use of Field Programmable Gate Arrays to implement the on-line event selection algorithms needed to achieve the highest capable accidental event rejection while keeping the trigger latency lower 400 ns. Resolutions on selection variables reconstruction are also presented.

I. INTRODUCTION

THE MEG experiment [1] operates a sensitive search for the $\mu^+ \rightarrow e^+ \gamma$ decay, a Lepton Flavour violating process, with a sensitivity on the branching ratio (10^{-13}) improved by two orders of magnitude with respect to the current limit[2]. This process is forbidden in the Standard Model of Particle Physics while it is foreseen to happen in a wide frame of Supersymmetric theories, whose predictions on that branching ratio lie in the range $10^{-14} \div 10^{-12}$. So an experimental proof of this signal would provide incontrovertible evidence in favour of Physics beyond the Standard Model.

This experiment utilizes the most intense, low energy DC muon beam, able to provide up to $10^8 \mu/s$, which is available at the Paul Scherrer Institut (PSI), Switzerland. The DC muon beam is produced by π^+ at rest on the 40 mm Carbon target of the proton beam (590 MeV/c, 2 μ Amp) and therefore the muon are monochromatics of 29 MeV/c. The beam also contains a background of 10^9 positrons that are effectively separated by an electrostatic separator and beam collimators. The beam, after the separator and an energy degrader, is stopped into a 180 μ m thick target. The event signature is given by a γ and a e^+ with energy equal to 52.8 MeV emitted at the same time and in opposite direction. The experimental apparatus combines different detection techniques, each one developed to achieve unprecedented performances at such energies. An 800 liters Liquid Xenon Calorimeter [3] provides γ detection. A magnetic spectrometer made of 16 Drift Chambers (DC) coupled to a quasi-solenoidal magnetic field performs e^+ tracking and 30 plastic scintillator bars (TC, [4]) are used for its timing. The expected resolutions are reported in Table I.

The predominant background of MEG comes from the accidental coincidence of a positron from an ordinary muon decay (called Michel positrons) with a gamma by a $\mu^+ \rightarrow$

TABLE I
EXPTECTED EXPERIMENTAL RESOLUTIONS

	FWHM
ΔE_e	$0.7 \div 0.9 \%$
ΔE_γ	4 %
$\Delta \theta_{e\gamma}$	$17 \div 20.5$ mrad
$\Delta T_{e\gamma}$	0.15 ns

$e^+ \nu_e \bar{\nu}_\mu \gamma$ or from a e^+ annihilation in flight. The second source of background, named correlated background, is the standard $\mu^+ \rightarrow e^+ \nu_e \bar{\nu}_\mu \gamma$ decay. Expected resolution will open the door to reach a single event sensitivity $\approx 5 \times 10^{-14}$ with 3×10^7 s of data taking, with an estimated background of ≈ 0.5 events.

The trigger system plays an essential role in processing the detector signals to find the signature of a $\mu^+ \rightarrow e^+ \gamma$ event in a severe pile-up environment performing a powerful background rejection, so to reduce the trigger rate below 10 Hz and keeping the lifetime $\geq 80 \%$ while preserving the efficiency on the signal $\epsilon \geq 95\%$. A constraint is imposed by the MEG waveform digitizers to the trigger system: must be shorter than the 500 ns depth of the digitizers cyclic memories [5]. Thus the trigger has to provide the Stop signal not later than 400 ns from the event occurrence. Finally it has to be flexible to accept other event types needed for detector calibration and monitoring.

This paper presents the architecture of the trigger system, the Firmware developed and its performance.

II. TRIGGER STRATEGY

The $\mu^+ \rightarrow e^+ \gamma$ signature for muon decay at rest in the laboratory is fully determined by two-body kinematics as written in Section I; it follows that useful observables to select events are energy of γ and e^+ , their time coincidence and opening angle. Requirement on the global trigger latency forces the system to use fast response detectors as the LXe calorimeter and the TC both read by PMTs and prevents us from using informations from the DC detector. The trigger algorithm discriminates on γ energy (E_γ), $e^+ \gamma$ time difference ($\Delta T_{e+\gamma}$) and their relative opening angle ($\theta_{e+\gamma}$).

The estimator E_γ is extracted from the pulse height of the sum of the LXe waveform. An on-line calibration taking into account PMTs gain, QE and geometric normalized is applied.

T_γ is obtained from a parabolic interpolation of the leading edges of the inner face PMTs. The algorithm selects the time of the PMT that collects the maximum amount of light. The same algorithm is applied the Timing Counter signals to

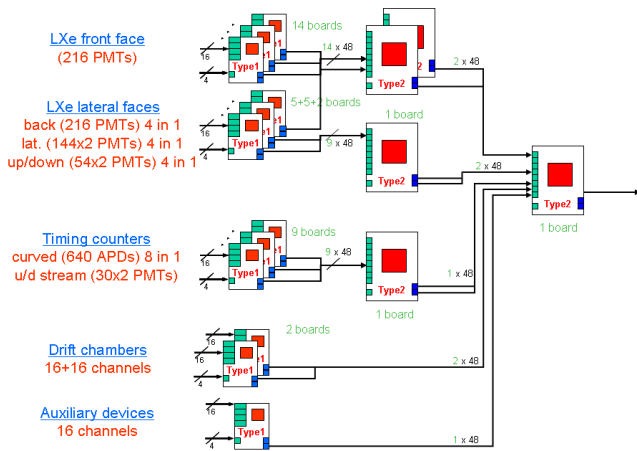


Fig. 1. Architecture of the trigger system

determine T_{e^+} estimator. The time selected corresponds to the first TC bar hit.

The impinging point of the photon onto the calorimeter and the TC crossing point of positrons provides an estimator of $\theta_{\gamma e}$. Impinging position of γ is given by the position PMT collecting the largest amount of light. The e^+ crossing position is given by the hit bar coordinate and the crossing position along the bars obtained comparing PMTs height pulses.

III. ARCHITECTURE

The Trigger system is arranged in a multi-layer structure, as shown in the Figure 1: a first layer hosts so-called Type1 boards which provides analog signals digitization and a second and a third layer with Type2 boards to collect Type1 data and operate selection algorithms. In addition, an Ancillary System was developed to ensure synchronous operation of the tree (data flux and algorithm execution). The logic is completely programmed into FPGAs and operates at 100 MHz frequency. The system consists in 40 Type1 boards, 6 Type2 and 4 Ancillary.

A. Type1 Board

Type1 boards are compliant with 6U VME standard. Each board receives 16 analog signals from experimental devices. These signals are digitized by means of 8 Flash ADC AD9218 [6], with 10 bit resolution and 100 MHz sampling speed. A Xilinx FPGAs Virtex-IIpro [7], [8], [9], receives digital data and operates first-level algorithms consisting in pedestal subtraction and calibration of all channels. The data transmission to second-level boards proceeds through LVDS serializers DS90CR481 [11], the transfer rate being 4.8 Gbit/s. Clock reference signal, distributed by Ancillary boards, is multiplied by a factor 5 and distributed all over the board by a Roboclock CY7B994V [12]. This chip provides an independent setting of skews with respect to the carrier signal, which is needed in order to synchronize FADC digitization, FPGA algorithm execution and data LDVS transmission.

1) *FE Electronics:* The differential input of Type1 FADCs is driven by an AD8138 [13] mounted on dedicated Front End boards. FE electronics is also capable to shift baseline value channel by channel in order to exploit the FADCs dynamic range. FE boards also operate an RC integration on input signals in order to improve on-line time estimation (see Section II); high frequency cut equal to 30 MHz is applied in LXe channels and 15 MHz on TC ones.

B. Type2 Board

Type2 boards are compliant of the 9U VME standard being used at the intermediate and top level of the trigger tree (see Figure 1). A Type2 receives up to 9 LVDS bus signals from lower level boards. Each LVDS bus is 48 bits wide and the translation from LVDS to CMOS signals is achieved by means of 48 bit deserializer DS90CR482, for a total data transfer rate of 4.8 Gbit/s. Data link to the upper level is guaranteed by 2 DS90CR481 serializer. Transferred data are processed by Xilinx Virtex-IIpro FPGAs. The algorithms processing is registered at 100 MHz. Clock signals are distributed by a Roboclock CY7B994V, as in the case of Type1 boards. The so-called Final Type2 collects the full information from the LXe and the TC to look for candidate events; if found, the Stop signal to the DAQ is asserted. In a similar way, the Final Type2 waits for clear of the Busy condition from all DAQ computers and generates a Start signal as soon as it happens. These signals are embedded in a control bus including other useful information for DAQ software, such as the event counter and trigger type.

C. Ancillary Board

Ancillary boards are a 9U VME board; they distribute the reference CLK and control signals (Start, Stop and Sync) to the entire Trigger System. The Ancillary System is arranged in a Master-Slave structure. The Master board hosts the reference CLK oscillator, a SARONIX SEL3935 [14] (19.44 MHz, jitter ≤ 30 ps over 100.000 cycles) and receives the control signals from the Final Type2 board. These signals are fanned-out through MAXIM LVDS [15] transmitters (maximum jitter ≤ 13 ps, skew ≤ 60 ps peak-to-peak over the 10 output) by 3 slave boards and distributed to all boards of the Trigger system. These are equipped with programmable delay generators for the distribution of control signals.

Proper trigger operation is guaranteed provided that algorithm execution on each board and data flow alongside the tree are synchronized. This is possible with a fine tuning of the skews of Roboclock CLK signals. We developed a tool to monitor the trigger synchronous operation: it checks both data transmission and memory addressing.

The system processes about 80 TB/s by means of all Type1 boards; the associated data transmission to the second layer is 30 GB/s.

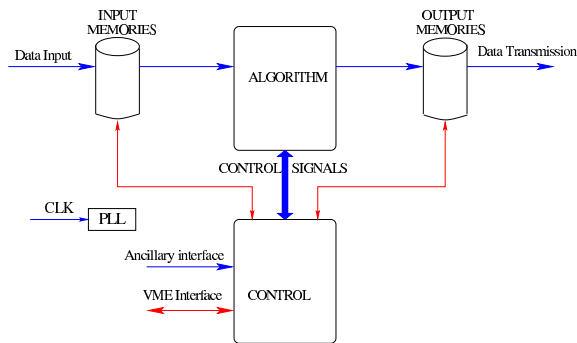


Fig. 2. FPGA firmware structure.

IV. ALGORITHM FIRMWARE

The trigger logic is implemented by the use of FPGAs. The choice of an FPGA-based digital trigger makes it versatile, as it is possible to operate different selection criteria by easily re-loading the configuration file onto the chip. The main frame of the logic is shown in Figure 2. The core consists in the algorithm block, which is specific of each board depending on its position in the trigger hierarchy and on the input detector signals to deal with. In all, 8 different versions of the firmware have been developed for Type1 boards and 5 for Type2.

Selection algorithms are implemented by using both combinatorial and sequential logic. More tricky operations (such as bus multiplication, waveform interpolation and so on), which would also require fuzzy or time-consuming logic, can be performed instead in 1 CLK cycle by resorting to RAM-based Look Up Tables (LUTs). These are widely used in our firmware, as in the case of PMT gain compensation or in the matching of relative $e^+ - \gamma$ direction patterns. Common to all firmware versions is a double stage of data storage, at the input/output of the algorithm block, which provides a powerful debugging tool to check both algorithm execution and board synchronization.

The system can generate up to 32 different trigger types ordered in a stack. The trigger for MEG signal events is assigned the highest priority, followed by MEG events with looser selection cuts. Trigger types used for single detector calibration and stability monitor are at the bottom of the stack. MEG events can be mixed with any other type with proper pre-scaling settings in order to compute signal efficiency and monitor detector stability during normal data acquisition. It is therefore desirable to program the fraction of each trigger type on a run-by-run basis. The content of each can be tuned by means of pre-scaling factors to be defined at the beginning of each run.

The choice of an FPGA chip as a platform follows the necessity of reducing the trigger latency as much as possible, which is mandatory in such a high-rate environment. By the use of a 100 MHz clock, we achieved an overall value ≈ 400 ns for the main $\mu^+ \rightarrow e^+\gamma$ trigger, including the time needed for data transmission through the trigger tree.

V. TRIGGER PERFORMANCES

The system is now operating at PSI during the first Physics run of the experiment. In this section results are shown for

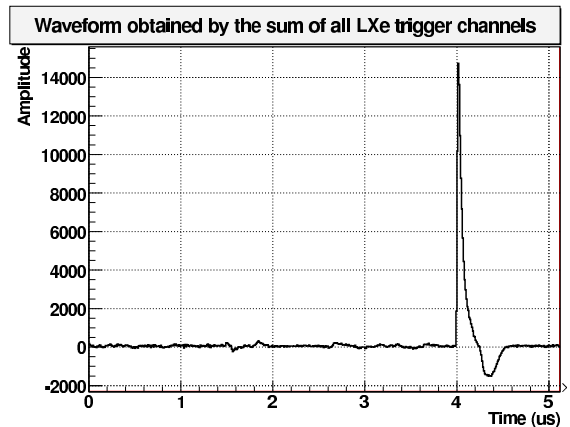


Fig. 3. Example of LXe summed waveform

the set-up of the $\mu^+ \rightarrow e^+\gamma$ trigger; an estimate of the trigger efficiency is provided for each observable being used. Resulting rates and livetime fraction are computed as well.

A. E_γ estimator

An efficient E_γ estimator is associated with the pulse height of LXe PMT signals, as resulting from the weighted sum of related waveforms. This requires an on-line calibration taking into account PMT+electronics gains, QE and PMT coverage. Daily basis PMT gain calibration are performed to check LXe stability and the results of calibrations, together with QE and geometrical factors, are loaded into a software programmable LUT. The sum over the 400 dedicated LXe trigger channels is obtained by mean of a scheme of 10 layers of parallel sum. Figure 3 shows an example of such a waveform, the E_γ on-line estimator is given by the height pulse of that waveform.

The Physics run followed a LXe calibration obtained with γ s from π^0 -decays induced by a beam of negative pions undergoing charge-exchange reaction $\pi^-p \rightarrow \pi^0n$ on a liquid Hydrogen target. Events were collected upon coincidence of LXe with a NaI tag-detector located at the opposite side, where the energy of the 2 γ is close to either edges (55 or 83 MeV) of the spectrum in the Lab frame. Lower energy γ s are particularly important as they allow us to study the LXe response function at an energy very close to the MEG signal. The on-line reconstructed spectrum obtained for those events in LXe is shown in Figure 4. With 9% FWHM resolution, it has been possible to set a threshold on E_γ discrimination at 45 MeV which guarantees an efficiency $\epsilon_{E_\gamma} \geq 99\%$. In first MEG physics run we decided to set a conservative threshold at 40 MeV because the LXe detector was not yet in a stable condition. The conditional probability of recognize a $\mu^+ \rightarrow e^+\gamma$ photon in analysis given a MEG trigger is shown in Figure 5 and is $\geq 99\%$ as expected.

B. Time Coincidence

The on-line time reconstruction is based on a parabolic fit of the rising edge of LXe and TC PMT waveforms. The rising edge of the PMT collecting the maximum light is chosen for T_γ and the sum of the waveforms of the hit bar for T_{e^+} . This is a good estimator of the time difference between γ s and e^+ s since the whole trigger system runs synchronously over LXe

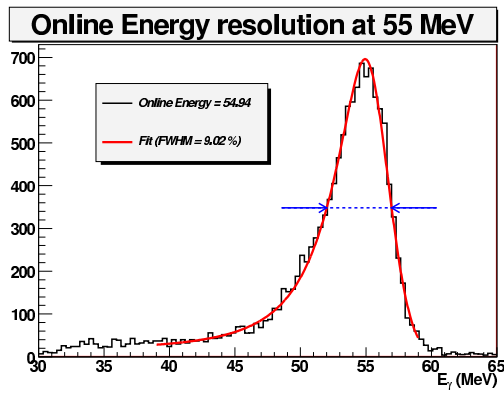


Fig. 4. On-line Energy resolution for a 55 MeV line

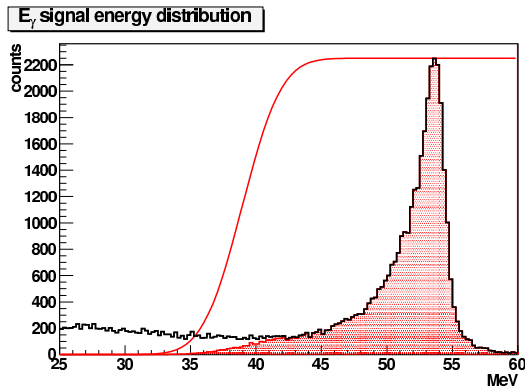


Fig. 5. Conditional efficiency of reconstruct a $\mu^+ \rightarrow e^+\gamma$ signal photon given a MEG trigger

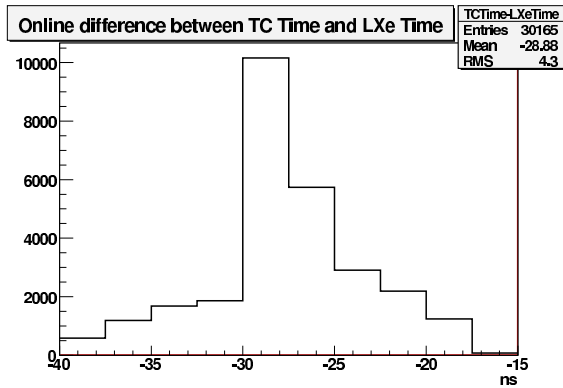


Fig. 6. On-line Energy Time Resolution

and TC channels. As presented in section III-C the ancillary system guarantees the global CLK to be distributed with a global jitter lower than 100 ps all over the channels. Online γ and e^+ timing needs to be calibrated according to the relative offsets, due to both cables and different algorithm latency, between the two detectors. To accomplish this task, the MEG experiment utilizes a proton beam delivered by a Cockcroft-Walton accelerator to induce radiative nuclear reactions on a boron-rich target, giving rise to an excited $^{12}\text{C}^*$ level which decays by emitting two cascade 4.4 and 11.7 MeV γ s. This provides an effective tool to study the relative timing of the two detectors. The resulting distribution is shown in Figure 6. The on-line resolution on $\Delta T_{e^+\gamma}$ turned out to be better than 4

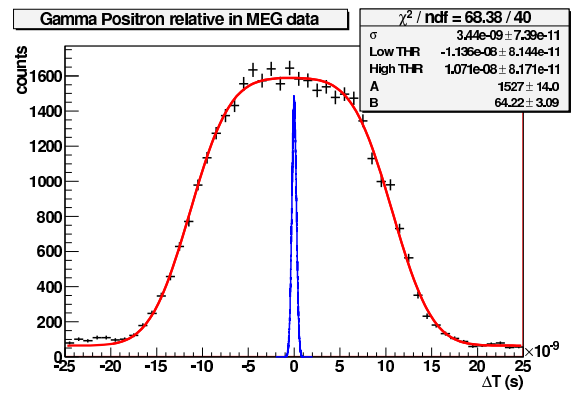


Fig. 7. ΔT distribution on MEG data given by trigger selection superimposed with signal shape

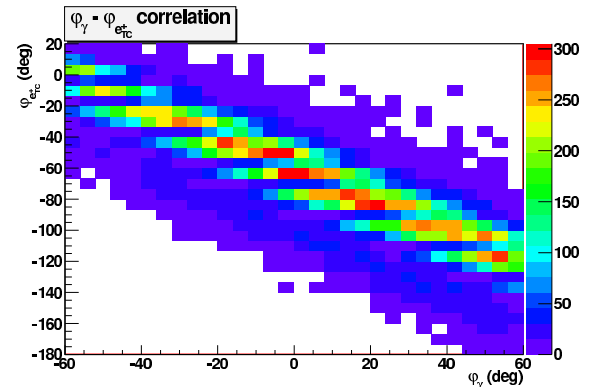


Fig. 8. Correlation between $\gamma_{\varphi_{LXe}}$ and $e^+_{\varphi_{TC}}$ in $\mu^+ \rightarrow e^+\gamma$ events

ns, while the offset was found to be 25 ns. This allowed us to set a 20 ns wide time-coincidence window, with an efficiency $\epsilon_{\Delta T_{e^+\gamma}} \geq 99\%$. This is confirmed by the off-line analysis. In Figure 7 is shown the off-line histogram distribution of $\Delta T_{\gamma e}$ and the PDF of $\mu^+ \rightarrow e^+\gamma$ signal superimposed. The centering of the window, its width, and on-line resolution on time difference are confirmed.

C. Direction Match

The long drift time of ionization electrons in the DC (of the order of a few hundreds ns) makes it incompatible with the request of short trigger latency and prevents us from using DC information for the reconstruction of positron direction at a trigger level. The selection of events with back-to-back $e^+ - \gamma$ pair is therefore based on the correlation between the impinging point of the γ on the calorimeter and of e^+ on the TC. In Figure 8 and 9 correlations between $\gamma_{(\varphi,z)_{LXe}}$ and $e^+_{(\varphi,z)_{TC}}$ are shown. Thus is possible to select back-to-back events based on that. The impinging point of the photon on the LXe is given by the PMT index in the inner face of the detector with the higher height pulse. This is obtained by means of a scheme of 8 layers of parallel comparators. For the e^+ the index of the hit bar is selected for φ direction, thus for z the logarithmic ratio of the height pulse of the PMT of hit bar is performed by means of LUTs. The designed project of the trigger system foresees to use a stereo readout of TC PMTs and dedicated fibers placed in front of the bars for z ,

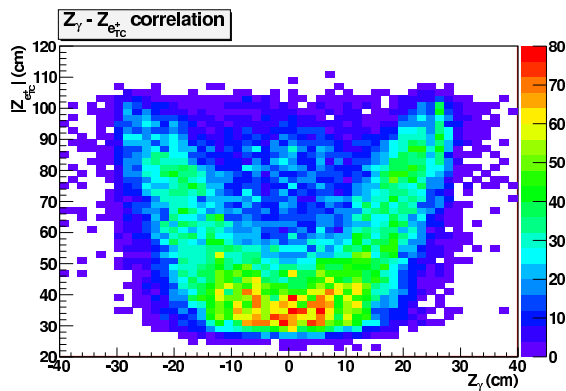


Fig. 9. Correlation between γ_{zLXe} and e^+_{zTC} in $\mu^+ \rightarrow e^+\gamma$ events

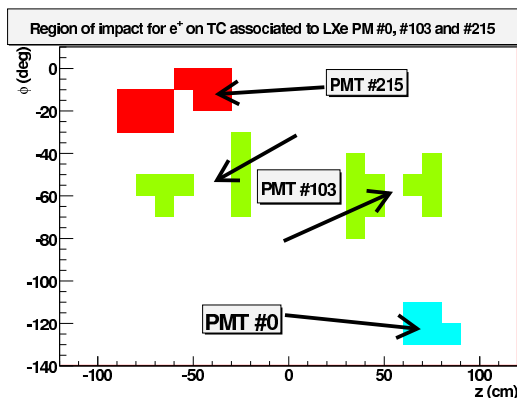


Fig. 10. Example of TC region impinged by a e^+ from $\mu^+ \rightarrow e^+\gamma$ decay in case of γ converting in front PMT #0 (top right corner of acceptance), PMT #103 (center of the acceptance), PMT #215 (bottom left corner of the acceptance) in the LXe calorimeter

but this system was not operative during the run. The use of the PMTs ratio causes us a lack of resolution on on-line z measurement. Figure 10 shows the 95% CL hit-domain for such a positron as predicted by MonteCarlo simulation for $\mu^+ \rightarrow e^+\gamma$ events for 3 different directions of the γ , which are reconstructed by the position of the PMT collecting the largest number of photoelectrons. For each LXe PMT index, a LUT returns a set of indices of TC sectors compatible with the hit-domain of a 52.8 MeV positron emitted backward. The direction condition is matched whenever a hit on the TC lies in this domain. The on-line resolution for this first physic runs had to be set at a value lower than the project of 95% because of the lack of z resolution measurement that should be compensated by enlarging the table of coincidence. This would lead to an improving of trigger rate and thus of the dead time. The best compromise between these two values leads to have an efficiency on direction match $\approx 66\%$.

D. Trigger rate, DAQ and livetime

As already stated in Section I, the MEG background is expected to be dominated by accidentals. If so, the $\mu^+ \rightarrow e^+\gamma$ trigger rate can be expressed by

$$R_{TRG} = R_\gamma \times R_{TC} \times f_\theta \times 2\Delta T \quad (1)$$

where (1) R_γ is the expected γ rate over threshold, R_{TC} the e^+ -hit rate on the TC, f_θ the rejection factor given by

direction match and $2\Delta T$ the time coincidence window. For a μ -stop rate = 3×10^7 , γ energy threshold = 45 MeV, $\Delta T = 10$ ns and 66% efficiency on $\theta_{\gamma e}$, R_{TRG} is expected to be ≈ 7 Hz. At the start of Physics run, September 2008, with the final configuration of $\mu^+ \rightarrow e^+\gamma$ trigger, we measured $R_{TRG} = 6$ Hz, close to expectation.

Data recorded on WFD cyclic memories are read-out by on-line DAQ clusters by means of the 2EVME transfer protocol. The deadtime per event of our DAQ system is approximately 40ms, corresponding to 83% livetime fraction, in agreement with experimental requests for the first physic run.

VI. CONCLUSIONS

The FPGA-based trigger of the MEG experiment is capable of performing a powerful background rejection with a 400 ns latency. The system is arranged in a multi-layer structure with 3 types of dedicated VME boards. The complete system is synchronous with a 100 MHz reference clock. On-line resolutions achieved on E_γ , $\Delta T_{e^+\gamma}$ and $e^+ - \gamma$ relative direction are compatible with the request of suppressing the background at the level ≈ 10 Hz, while keeping the overall efficiency above 90%.

The system was operative since 2007 and data presented in this article refers to 2008 physics run. The behaviour of the system is compatible with expectation. The hardware failure of the TC fiber system causes a lack of resolution on positron direction measurement preventing the system to reach the foreseen 90% efficiency on $\mu^+ \rightarrow e^+\gamma$ selection.

REFERENCES

- [1] Baldini et al, The MEG Experiment: search for $\mu^+ \rightarrow e^+\gamma$ decay at PSI, Proposal to INFN, September 2002.
- [2] MEGA Collaboration, Phys. Rev. D **65** (2002) 112002 <http://arxiv.org/abs/hep-ex/0111030>.
- [3] A. Baldini et al., "Liquid Xe scintillation calorimetry and Xe optical properties" <http://arXiv:physics/0401072>.
- [4] MEG Collaboration, "MUEGAMMA timing counter prototype test", PSI Annual Report (2001)
- [5] S. Ritt, contribution to the IEEE 2004 Conference, Nuclear Science Symposium available at http://ieeexplore.ieee.org/xpls/abs_all.jsp?arnumber=1462369
- [6] Analog Devices, AD9218, 10 bit 3V Dual A/D converter, <http://www.analog.com>
- [7] See documents and informations available at <http://www.xilinx.com>
- [8] Xilinx, "Virtex II Pro and Virtex II Pro X FPGA user's guide", UG12(v3.0) (2004) available at <http://www.xilinx.com>
- [9] Xilinx, "Virtex II Pro Platform FPGAs: Complete Data Sheet", DS083 (2004) available at <http://www.xilinx.com>
- [10] Xilinx, "Virtex II Pro Platform FPGAs: Complete Data Sheet", DS083 (2004) <http://www.xilinx.com>
- [11] DS90CR481/DS90CR483 48-bit LVDS Channel Link SER/DES-65-112 MHz, <http://www.national.com>
- [12] Cypress, High-speed Multi-phase PLL clock Buffer, <http://www.datasheetcatalog.com>
- [13] Analog Devices, AD8138, Low Distorsion Differential ADC driver, <http://www.analog.com>
- [14] SaRonix, Crystal Clock Oscillator, <http://www.pericom.com/saronix>
- [15] Maxim, Low-Jitter 800 Mbps 10-Port LVDS Repeaters, <http://www.maxim-ic.com>